What is claimed is:

1. A semiconductor device formed on a semiconductor substrate, said semiconductor device comprising:

an active region formed on the semiconductor substrate;

a dummy active region formed on the semiconductor substrate in a rectangular shape, wherein a length of a short side of said dummy active region is substantially no greater than 1μm and more than 0.5μm, wherein a distance between said active region and said dummy active region is greater than 0.5μm and less than 10μm; and

an isolation region formed on the semiconductor substrate and surrounding said active region and said dummy active region.

2. A semiconductor device according to claim 1, wherein said isolation region includes a trench filled with a high density plasma chemical vapor deposition layer.

3. A semiconductor device according to claim 2, wherein a depth of the trench is about 2500 Å to 5000 Å.

4. A semiconductor device according to claim 2, wherein the trench has a tapered shape.

5. A semiconductor device according to claim 2, wherein a taper angle of the trench is about 70 to 90 degrees.

6. A semiconductor device according to claim 2, wherein the high density plasma chemical vapor deposition layer is an oxide film.

7. A semiconductor device according to claim 6, wherein the oxide file is abraded by Chemical Mechanical Polishing (CMP).

8. A semiconductor device according to claim 4, wherein a width of an opening of the trench is wider than a width of a bottom of the trench.

9. A semiconductor device according to claim 8, wherein the width of the opening of the trench is 0.5 to 1 μm.

10. A semiconductor device formed on a semiconductor substrate, said semiconductor device comprising:

an active region formed by the semiconductor substrate;

a dummy active region formed on the semiconductor substrate in a rectangular shape, wherein a length of a short side of said dummy active region is substantially no greater than 1μm and more than 0.5μm, wherein a distance between said active region and said dummy active region is greater than 0.5μm and less than 10μm;

an isolation region formed on the semiconductor substrate and surrounding said active region and said dummy active region; and

a semiconductor element formed on said active region, said semiconductor element including a gate electrode formed over said region, wherein a distance between said dummy active region and said gate electrode is more than 0.5μm.

11. A semiconductor device according to claim 7, wherein said isolation region includes a trench filled with a high density plasma chemical vapor deposition layer.

12. A semiconductor device according to claim 11, wherein a depth of the trench is about 2500 Å to 5000 Å.

13. A semiconductor device according to claim 11, wherein the trench has a tapered shape.

14. A semiconductor device according to claim 11, wherein a taper angle of the trench is about 70 to 90 degrees.

15. A semiconductor device according to claim 11, wherein the high density plasma chemical vapor deposition layer is an oxide film.

16. A semiconductor device according to claim 15, wherein the oxide film is abraded by Chemical Mechanical Polishing (CMP).

17. A semiconductor device according to claim 13, wherein a width of an opening of the trench is wider than a width of a bottom of the trench.

18. A semiconductor device according to claim 17, wherein the width of the opening of the trench is 0.5 to 1 μm.